

# EXPERIMENT NO: 12

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## Aim of the Experiment:

Analysis of Full Adder using eSim.

## Theory :

The full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry. When a full adder logic is designed we will be able to string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next.

A full adder circuit can be implemented with the help of two half adder circuits. The first will have the half adder to add A and B to produce a partial Sum. The second half adder logic can be used to add input carry to the Sum produced by the first half adder to get the final sum output. If any of the half adder logic produces a carry, there will be an output carry.

## Procedure:

1. Create the schematic of the Full Adder as shown in Figure-1.
2. Annotate the schematic.
3. Test Electric rules.
4. Generate the netlist.
5. Insert analysis for transient analysis from 0 to 100 sec with a step time of 10 sec.
6. Insert Source Details.
7. Add full\_adder.sub Subcircuit file in Subcircuit Tab for Full Adder.
8. Convert KiCad netlist to Ngspice netlist.
9. Simulate the Ngspice netlist using Ngspice simulator.

## Source Parameters:

For DC Voltage Source (V1):

1. Enter Value for V1 - 5

For DC Voltage Source (V2):

1. Enter Value for V1 - 0

For DC Voltage Source (V3):

1. Enter Value for V1 - 5

## Schematic Diagram:

The circuit schematic of full adder in eSim is as shown below:

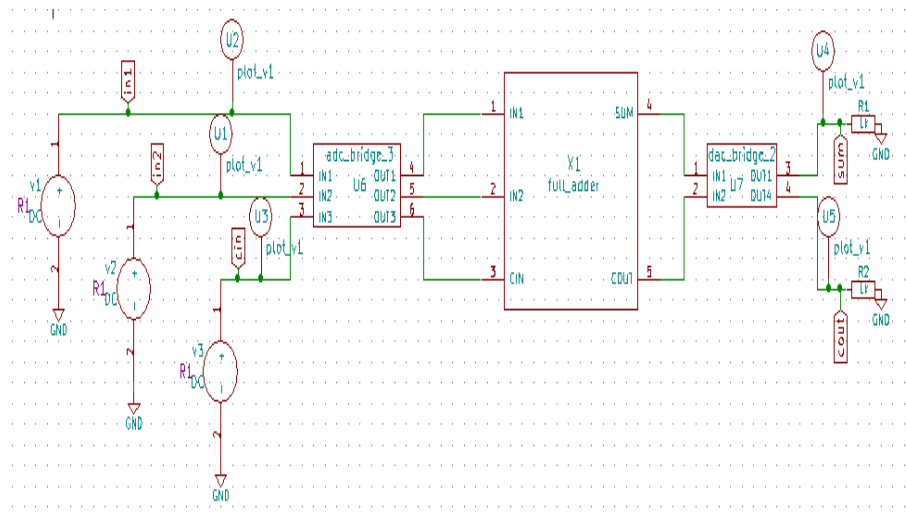


Figure 1: Full adder

## Simulation Results:

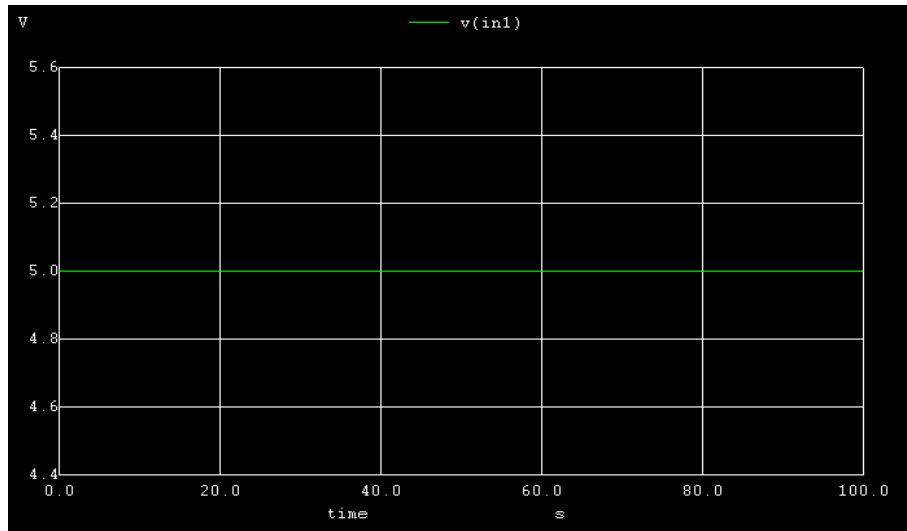


Figure 2: Ngspice Input-1 Plot

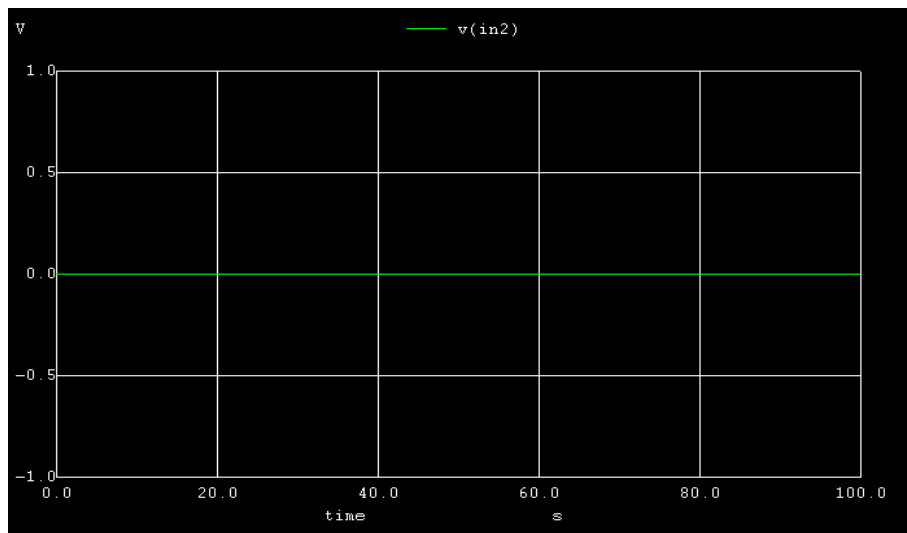


Figure 3: Ngspice Input-2 Plot

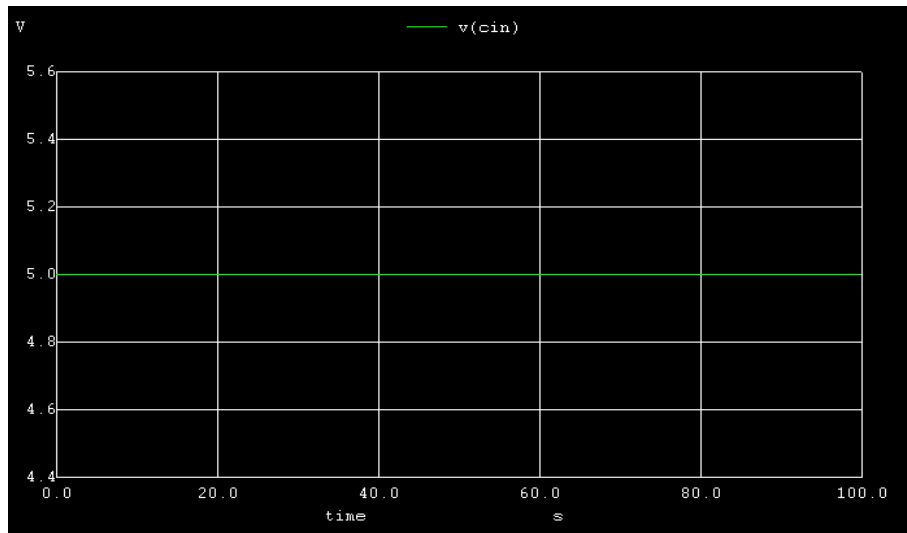


Figure 4: Ngspice Input Cin Plot

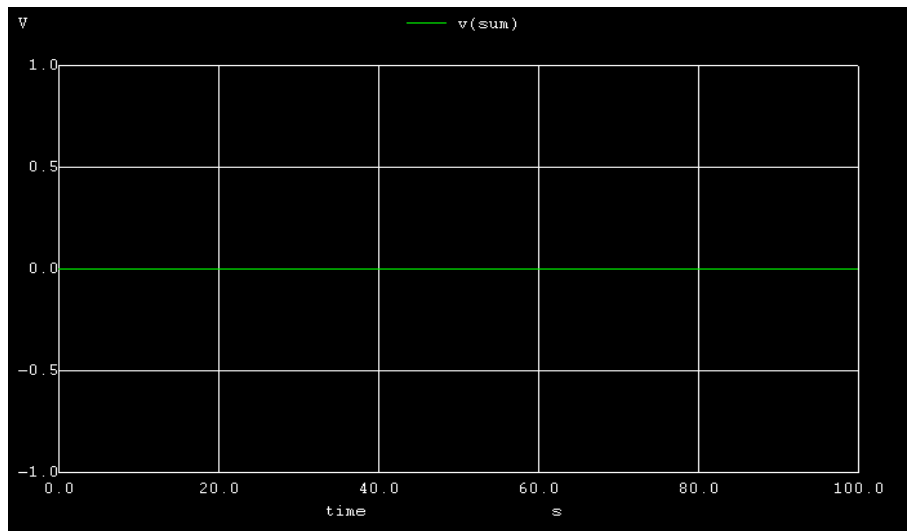


Figure 5: Ngspice Output Sum Plot

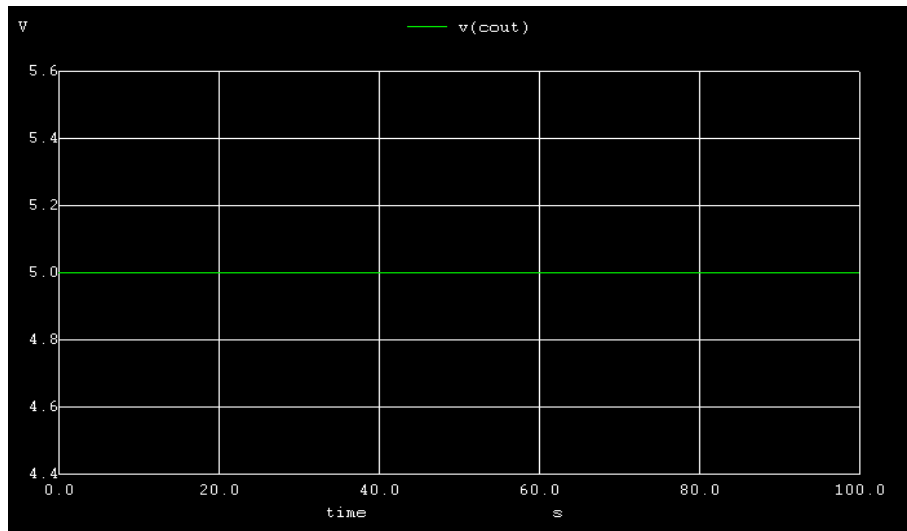


Figure 6: Ngspice Output Carry Plot

## Conclusion:

Thus, we have studied the full adder using eSim and we get the appropriate waveforms.

## References:

<http://www.circuitstoday.com/half-adder-and-full-adder>